Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROYUKI MIZUNO, TAKAHIRO NAGANO and YOSHINOBU NAKAGOME

Appeal No. 2000-0452
Application No. 08/622,389

ON BRIEF

Before HAIRSTON, LEVY, and LALL, Administrative Patent Judges

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1, 3 to 18 and 22[1], all the pending claims in the application.

[1] Both the examiner and the appellants have stated that claims 1 and 3 through 22 are on appeal. However, due to the entry of an amendment filed on October 19, 1999 (paper no. 27) and its entry on November 29, 1999 (paper no. 28), claims 19 through 21 have been canceled. Therefore, only claims 1, 3 to 18 and 22 are pending in this application.

According to appellants, the invention is directed to a circuit, and a microcomputer including the circuit, by controlling power consumption of a semiconductor device by controlling the subthreshold leakage current in response to the frequency of a reference signal. The subthreshold leakage current is controlled by controlling the threshold voltage of transistors of the semiconductor device.

The following claim is illustrative of the invention:

1. A semiconductor integrated circuit comprising:

> a logic circuit which implements a certain logical processing, the logic circuit including a unit logic circuit having two inputs and one output;
>
> a control circuit which controls the threshold voltage of transistors that constitute said logic circuit; and
>
> a first circuit whose delay characteristics can be controlled,
>
> said transistors of said logic circuit comprising MIS transistors, said first circuit delivering an output signal to said control circuit which also receives a reference signal, said control circuit producing a first and second control signals correspondent with said reference signal, said first control signal being fed to said first circuit, and said second control signal being fed to said MIS transistors of said logic circuit so as to vary power consumption and operation speed of said logic circuit in response to a frequency of said reference signal.

The examiner relies upon the following references:

Tomisawa	5,039,893	Aug. 13, 1991
Nakajima et al. (Nakajima)[2]	JP 62-272619	Nov. 26, 1987
Kamisaka et al. (Kamisaka)	JP 05-235714	Sep. 10, 1993

Chen et al. (Chen), "A High Speed SOI Technology With 12ps/18ps Gate Delay Operating at 5V/1.5V", IEDM Technical Digest, pp. 35-38 (1992).

Claims 1, 3 through 12, 14 through 18 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Nakajima in view of Tomisawa and Chen.[3]

Claims 1 and 3 through 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Nakajima in view of Kamisaka and Chen.

Rather than repeat the arguments of appellants and the examiner, we make reference to the brief (paper no. 22), reply brief (paper no. 25) and the examiner's answer (paper no. 24) for the respective details thereof.

---

[2] Our understanding of the Japanese references (Nakajima and Kamisaka) is based upon the English translation provided by the PTO Translation Branch, copies of which are enclosed with this decision. Regarding the Nakajima reference, it is noted that on page 1 of the English translation, the name Nakashima appears instead of Nakajima. However, since the Serial no. of the Japanese copy and the English translation match as do the figures in the translation and the Japanese patent, we are of the view that the translation is indeed the translation of the Nakajima patent, and that Nakashima is mistakenly stated instead of Nakajima.

[3] The examiner has apparently by typographical error included claims 19 through 21 in the above rejections. However, claims 19 through 21 have been canceled. See paper nos. 27 and 28.

OPINION

We have considered the rejections advanced by the examiner and the supporting arguments. We have, likewise, reviewed the appellants' arguments set forth in the briefs.

We reverse.

As a general proposition, in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness, is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

Appellants argue (brief at page 6) that "[a]lthough Kamisaka [or Tomisawa] teaches a logic unit . . ., there would be no motivation to combine these two references in the manner asserted

absent Appellant's teaching regarding the control of power consumption and operation speed of the logic circuit" (brief at pages 6 and 7).

The examiner asserts (answer at page 4) that "it would have been obvious . . . to employ the teaching of Tomisawa to control the delay time of other logic circuits . . . so that the control of all the transistors on the same substrate could be uniform and [all the transistors] are subject to similar process variations, thus, the delay time for all the logic circuits could be controlled similarly." The examiner further asserts in response to the lack-of-motivation argument (answer at page 9) that "the combination is based on the teachings of Tomisawa and Kamisaka to control the delay time of other logic circuits in a similar manner as the oscillator of Tomisawa and the delay of Kamisaka are controlled."

In providing motivation or a suggestion to combine, we note that the Federal Circuit states, in In re Lee, 277 F.3d 1338, 1342-43, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002),

> [t]he essential factual evidence on the issue of obviousness is set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966) and extensive ensuing precedent. The patent examination process centers on prior art and the analysis thereof.

> When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. See, e.g., McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the Graham factors).

Having reviewed the statement of obviousness in these rejections, the examiner-advocated motivation to make the combination and the examiner's response to arguments by appellants for lack of motivation, we find no factual basis or motivation for suggesting the combination as suggested by the examiner. We find that each of the Nakajima, Kamisaka and Tomisawa reference is concerned with the operation of a delay circuit and changing the circuit operation in response to a reference signal. None of these references suggests or teaches that Nakajima could be combined with either Tomisawa or Kamisaka. Therefore, we agree with appellants' position that there is no motivation as required by Lee, supra, to combine Nakajima with Tomisawa or Kamisaka, there being no argument regarding the teachings of Chen regarding the use of MIS transistors in place of MOS transistors in the formation of the delay circuits.

Even if the references were to be combined, arguendo, we still find that Nakajima combined with either Tomisawa or Kamisaka and Chen does not meet the recited limitations of claim 1. For example, the examiner has not pointed out how the combination of Nakajima and Tomisawa, or the combination of Nakajima and Kamisaka yields the recited control circuit producing first and second control signals wherein said first control signal is fed to "said first circuit", and said second control signal is fed to said "MIS transistors of said logic circuit." Therefore, we are of the view that the examiner has not produced a prima facie case of obviousness by combining Nakajima with either Tomisawa or Kamisaka, noting that the addition of Chen contributes nothing to the electrical configuration of the circuit claimed.

With respect to the other independent claims, 3 and 14, we note that they each have the same or similar recited limitations.

Regarding independent claim 8, we find the examiner has not shown how the combination of Nakajima and Tomisawa or Nakajima and Kamisaka shows the recited limitation "said control circuit receives said reference clock signal and controls said oscillation circuit with said control signal so that the

oscillation frequency of said oscillation circuit corresponds with the frequency of said reference clock signal." The examiner responds (answer at pages 11 and 12) that "[i]t is notoriously well known in the art that a reference clock can be generated by a voltage controlled oscillator to provide a stable clock signal. . . . Thus, it would have been obvious . . . to generate the reference clock (a) of Nakajima with a voltage controlled oscillator to provide a stable clock signal to minimize any jitter in the signal, thereby having the reference clock signal frequency determined by an input of the voltage controlled oscillator." We find that, while it may be notoriously well known to change the frequency of an oscillator by using a reference clock signal, the examiner's response does not address the interaction of the control circuit with the oscillation circuit in the manner recited in the above quoted limitation. Therefore, we are of the view that the examiner has not made a prima facie case of obviousness in rejecting claim 8.

Having found the rejections of all of the independent claims 1, 3, 8 and 14 as untenable, we also do not sustain the rejection of dependent claims 4 through 7, 9 through 13, 15 through 18 and 22 over Nakajima in view of Tomisawa or Kamisaka, and Chen.

Accordingly, the decision of the examiner rejecting the claims under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
PARSHOTAM S. LALL Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)	

vsh

FAY, SHARPE, BEALL, FAGAN
MINNICH & MCKEE
104 EAST HUME AVENUE
ALEXANDRIA, VA 22301